XPEEDIC
ACCELERATE YOUR IC DESIGN

Heracles

Automated High-Speed PCB Design SI Sign-Off

Highlights

1. Signal integrity sign-off becomes critical for high speed PCB designs. Traditionally 3D EM solver is expensive to run such a simulation, especially scan the board to identify any violation for the sign-off purpose.

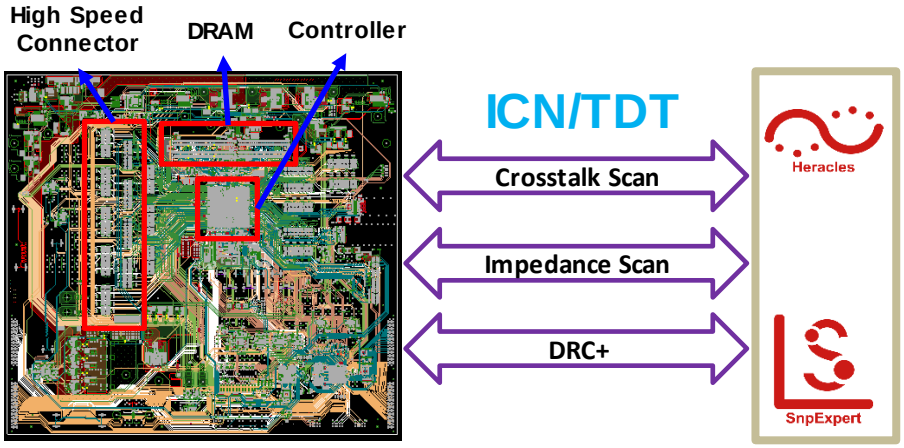
2. Heracles enables SI engineers to scan the via pin field and breakout region under connectors or BGA packages for impedance and crosstalk violation with its novel full-wave solver technology which has the same accuracy as the traditional 3D solver but an order of magnitude faster.

3. Crosstalk metrics such as frequency domain integrated crosstalk noise (ICN) or time domain waveform TDT are derived from the S-parameter to quantify crosstalk.

4. Heracles's Impedance Scan flow can quickly check geometry and electrical design rules, which can improve working efficiency.

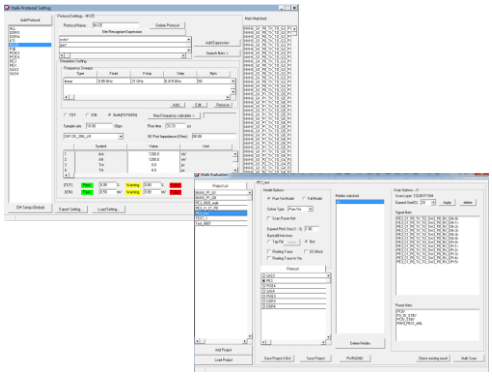
What can Heracles do?

- Heracles enables SI engineers to scan the via pin field and breakout region under connectors or BGA packages for impedance and crosstalk violation with its novel full-wave solver technology which has the same accuracy as the traditional 3D solver but an order of magnitude faster.



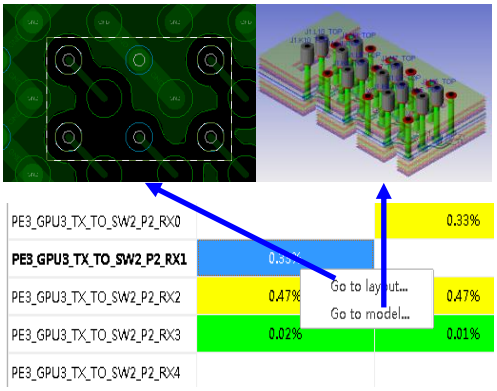
Crosstalk Scan

- The Crosstalk scan can automatically extract selected nets in the via pin field and breakout region under connector or BGA package base on user configuration of the high speed interface definition.



Quick Issue Identification

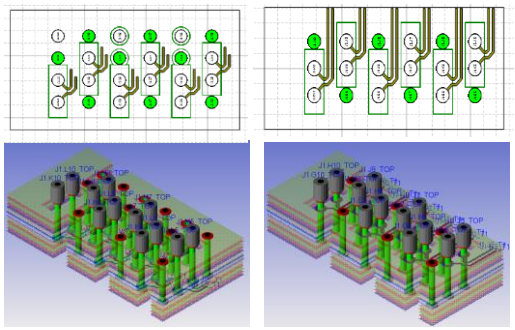
- The crosstalk metrics such as ICN/TDT allow quick assessment of the crosstalk by simply comparing. It also maps to the **Layout** and **ViaExpert** with different colors to allow quick location identification.

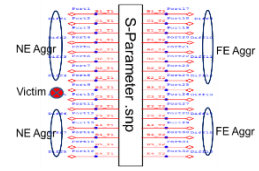


EM solvers and Crosstalk Metrics

- Three solvers are available in Crosstalk Scan flow: FEM3D, Hybird Solver and Pure Via Solver .To get controllable accuracy and speed, Pure Via Solver is recommended in Crosstalk Scan flow and Hybird solver is applied in Impedance Scan flow.
- Frequency domain integrated crosstalk noise (ICN) or time domain waveform TDT can be used to quantify crosstalk, NEXT and FEXT.

Pure Via Model **Full Model**

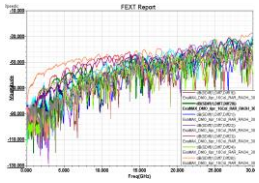


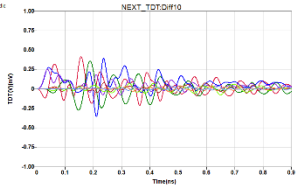


$$\sigma_x = \sqrt{\sigma_{nx}^2 + \sigma_{fx}^2}$$

$$\sigma_{nx} = \left(2\Delta f \sum_n W_{nt}(f_n) 10^{-MDNEXT_{loss}(f_n)/10}\right)^{1/2}$$

$$\sigma_{fx} = \left(2\Delta f \sum_n W_{ft}(f_n) 10^{-MDFEXT_{loss}(f_n)/10}\right)^{1/2}$$

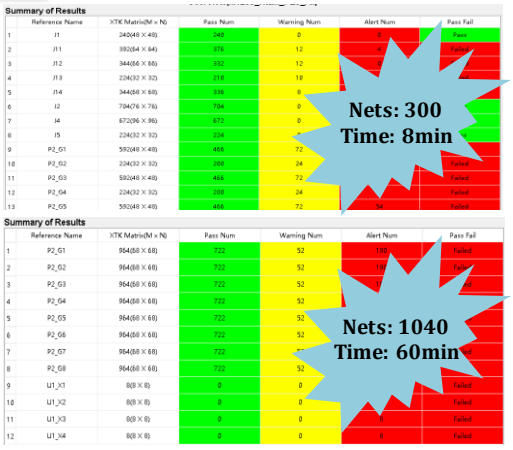




Crosstalk Scan Flow

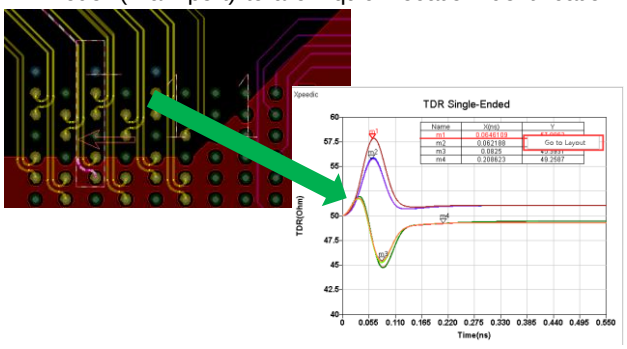
- The crosstalk scan first starts with the signal net scanning based on the user configuration of the high speed interface definition.
- The selected nets in the via pin filed and breakout region under connector or BGA package are automatically extracted without user intervention.
- The resultant crosstalk level for the selected nets is shown in either table or plot format.

Define protocols → 1. Scan board 2. Select protocol, ref des, nets → 1. Create EM Models for each crosstalk group 2. Distribute the EM jobs → 1. Collect S-parameter and post-process 2. Generate crosstalk table



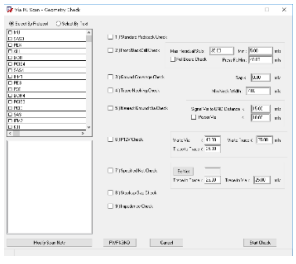
Impedance Scan Flow

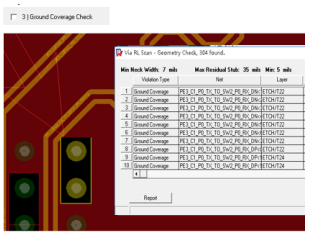
- Heracles's Impedance Scan flow can quickly check geometry and electrical design rules, which can quickly finds any outlier(s) if there is any.
- Support map to Cadence layout and Xpeedic 3D model (ViaExpert) to allow quick location identification.



DRC+

- Geometry Check (DRC+) can perform additional checks on top of Cadence Allegro.
- Standard pad-stack, back drill, ground coverage, trace necking, nearest ground via, power plane, specified net(s) can be checked in a blink.
- Support to identify the violation in Cadence Allegro and generate report.





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