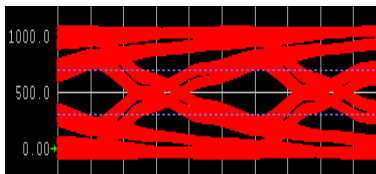
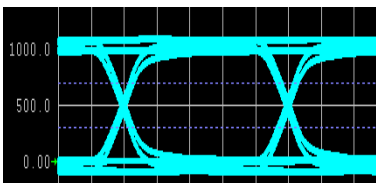


From this....



To this....



*A 2-day advanced training class with
Dr. Eric Bogatin, Signal Integrity Evangelist*

AGCD: Advanced GigaBit-Differential Channel Design

Open your eyes by optimized interconnect design

Now with hands on labs!

Are you designing one of the alphabet soup high speed serial links like PCIe, SATA, SAS, XAUI, GigE, USB or LVDS? Then all of your interconnects are differential pairs and eliminating signal integrity problems in your design will determine whether your product works or not.

This 2-day, advanced training class will bring you “up to speed” on how to design the physical interconnects of your channel to improve signal quality and achieve the bit rate you need. We eliminate the myth-conceptions that dominate the industry and show you the right way of designing differential pairs that operate above 15 Gbps.

We eliminate the confusion over:

• Tight or loose coupling	• Transparent via design
• Differential mode vs odd mode impedance	• Mode conversion and length matching
• Conductor loss and copper roughness	• S-parameters without tears
• Dielectric loss	• The limits to FR4

Now with hands on labs!

The most common answer to all signal integrity questions is “it depends”. The way we answer it depends questions is by putting in the numbers. While this class introduces many rules of thumb and approximations, sometimes, to get a good answer requires a simulation. This is why numerical simulation tools are essential.

By special arrangement, we give you access to Mentor Graphics HyperLynx to run hands on labs we created specifically for this class. These labs illustrate the design principles and allow you to explore design space with virtual prototypes, on your own, after the class.

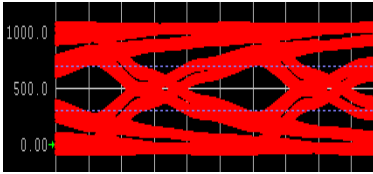
No previous simulation experience is necessary. Even if you have never done any simulation before, you will find the labs we have created easy to use and help you immediately apply the principles you learn in class to your next design.



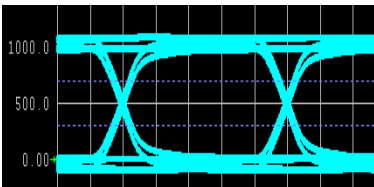
How Do I Register?

Online at www.beTheSignal.com,
info@beTheSignal.com for questions and group discounts.
Schedule is online at www.beTheSignal.com

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Open your eyes by optimized interconnect design

Class Outline

Day 1

Day 2

<p>01 Opening Eyes by Optimized Interconnect Design</p> <ul style="list-style-type: none"> • The design process • ISI and eye collapse: 4 sources • Jitter from PDN noise • All interconnects are differential • 4 types of simulation 	<p>05 Discontinuities</p> <ul style="list-style-type: none"> • Using S-parameter models of connectors, etc. • Approximating as transmission lines • Does location matter- losses as your friend • Three design guidelines to minimize impact • Features and maximum data rate
<p>02 Differential Pairs and Routing</p> <ul style="list-style-type: none"> • Differential impedance and stack up design • Tight or loose coupling? • Differential circuits and termination • Routing stubs and max data rate • Other stubs and maximum data rate 	<p>06 Transparent Via Design</p> <ul style="list-style-type: none"> • Four via features and their impact • Via to via coupling and role of the cavity • Simple models for vias • Mode conversion • Optimized via design
<p>03 Channel to Channel Crosstalk</p> <ul style="list-style-type: none"> • NEXT, FEXT • Worst case FEXT, NEXT • Role of coupling • Return path discontinuities and ground bounce • Important design rules to reduce crosstalk 	<p>07 Lossy Lines and ISI</p> <ul style="list-style-type: none"> • Rise time degradation and ISI • Losses and jitter • Root cause of rise time degradation • Estimating losses and highest data rate • Introduction to equalization
<p>04 Mode Conversion</p> <ul style="list-style-type: none"> • Root cause • Why do we care: the three big reasons • Length compensation and glass weave • From cross talk • Practical considerations 	<p>08 Practical Considerations</p> <ul style="list-style-type: none"> • The five most important design guidelines • S-parameter analysis of a channel • Finding the root cause • SDA: Jitter decomposition • Understanding channel specifications

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