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Dielectric Estimation and Laminate Analysis Method (DELAM) TEST METHOD

Document Number: PWB 6137	
Subject Dielectric Estimation and Laminate Analysis Method (DELAM)	
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1.0 Scope

This test protocol measures changes in capacitance of printed-wiring board (PWB) substrates both before and after assembly, rework and/or thermal shock. Exposing a test vehicle to increasing numbers of cycles and temperatures experienced during the assembly environment creates thermal stressing. Measured changes in bulk capacitance represent potential risk that the PWB's base materials have delaminated

Additional analysis of measured data can also be used to verify and validate the product construction and characterize properties associated to dielectric constant.

This technique requires a specifically designed test coupon, which contains interconnections to each internal layer designed as a power/ground plane. Design files are available upon request from PWB Interconnect.

Thermal excursions can also be re-produced by the IST Preconditioning application using a DC current to heat the coupons (IPC TM650 2.6.26).

Detailed information regarding how to determine the product construction and characterization of material properties are available upon request from PWB Interconnect Solutions Inc.

2.0 Applicable Documents

2.1 IPC TM650 2.5.2 Capacitance of Insulating Materials
2.2 IPC TM650 2.5.5.1 Permittivity and Loss Tangent of Insulating Material at 1 MHz
2.3 IPC-TM-650, Method 2.1.1, Microsectioning
2.4 IPC-TM-650, Method 2.1.1.2, Microsectioning - Semi or Automatic Technique

3.0 Test Specimens IST DELAM test coupon per Figure 4. See Paragraph 8

4.0 Apparatus or Material

4.1 Capacitance Meter with Kelvin Capability

4.2 Two, Kelvin probes

5.0 Procedure

5.1 Sample preparation

5.1.1 Each coupon should be serialized with unique part number, to ensure traceability.
5.1.2 Create a spreadsheet to include all as received coupon data, for used in subsequent analysis and comparison. The input information should/could include;
a) Four-wire resistance measurements for each traditional IST test circuit. Using micro-ohm meter, electrically prescreen and record bulk resistance for each test circuit
b) Registration data. Using continuity meter measure and record registration data.
c) Initial capacitance values, for each pair of adjacent vias. Using capacitance meter, follow the protocol in paragraph 5.2.

Note: This procedure will be repeated for each coupon's condition (As Received, after each cycle of assembly/rework or after IST preconditioning).

5.2 Capacitance Measurement Procedure

5.2.1 Allow test equipment 30 minutes to warm up and stabilize.

5.2.2 Confirm equipment accuracy with in-house calibration procedures, device and/or standard.

Test Conditions	PWB Measurement Range	Typical Set-up
Frequency	300 KHz - 1 MHz	1 MHz
Accuracy	+/- 0.5%	+/- 0.5%
Range	100 Pf – 1000 Pf	400 Pf
Test Temp °C	23°C +/- 3°C	23°C
Test Temp °F	(73°F +/-5°F)	73°F

5.2.3 With the coupons oriented with via identifications in numerical order with the lowest connected layer on the left hand side, probe/measure the first two adjacent vias and record the capacitance values into the spreadsheet.

5.2.4 Continue to measure and record each pair of adjacent vias, in sequence (E.g. 1 to 2, 2 to 3, 3 to 4, Etc.), until complete.

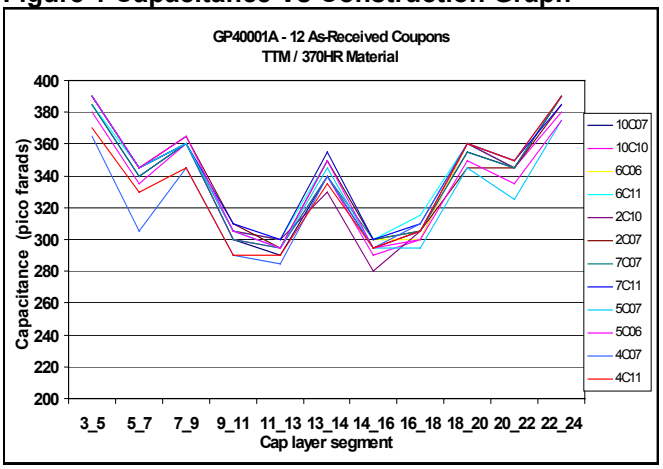
5.2.5 Repeat procedure for all coupons.

5.2.6 Analyze collected data for any measurement anomalies; repeat step 5.2.3 to confirm for correctness.

5.2.7 Statistically and graphically compare data for consistency.

5.2.8 Initial analysis should establish a reference for subsequent measurements completed after each thermal excursion (Assembly, Rework, IST Preconditioning, Etc.), using steps 5.2.3 through 5.2.6. An example of a graphical comparison of as received data is shown in Figure 1.

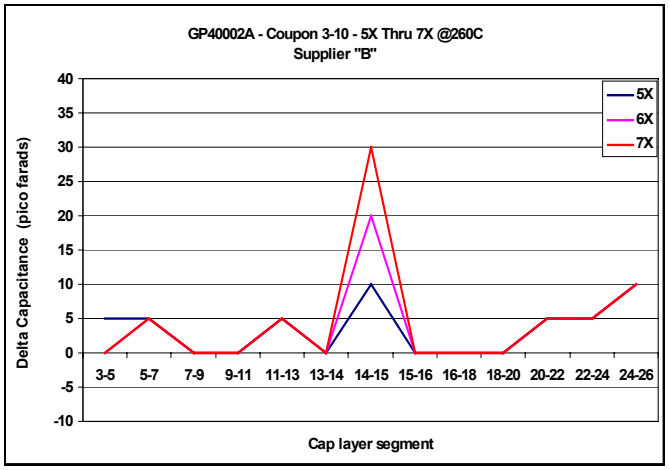
Figure 1 Capacitance Vs Construction Graph



5.3 Comparative Analysis

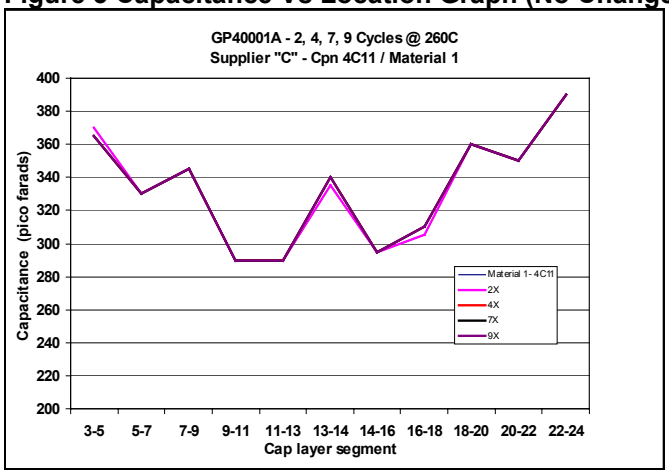
5.3.1 Each coupon's data should be statistically and/or graphically compared to identify changes in measured values. Figure 2 illustrates the delta in capacitance values related to 3 sequential thermal cycles. The increasing positive delta is indicative of material delamination. Values increasing from 10 to 30 Pico-farads in the central location are signifying a relative change, especially when all other readings remain unchanged.

Figure 2 Change in Capacitance Vs Location Graph



5.3.2 Figure 3 demonstrates the absolute values for a coupon that experienced up to 8 cycles of assembly without a minimal measured change in capacitance.

Figure 3 Capacitance Vs Location Graph (No Change)



6 Microsection Evaluation

6.1 If increased capacitance values (more than 2.5% higher) are measured between the as received and thermally stressed coupons failure analysis should be completed to confirm the magnitude and exact location of the delamination condition. Microsection of failed coupons shall be performed in accordance with IPC-TM-650, Method 2.1.1 or 2.1.1.2.

7 PROTOCOL DETAILS

Additional information is available from:
PWB Interconnect Solutions Inc.
235-103 Stafford Rd West
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8 IST DELAM Coupon.

The test coupon is incorporated onto the production panel to monitor or qualify design, materials or process and provide risk assessment of product and/or reliability assurance

The IST coupon enables measurements between each internal reference (power/ground) plane. The modification will not affect the existing circuits, connectors or registration areas. The required changes are located along one edge of the design, between the outside row of vias and the edge/profile of the coupon.

A series of .040” drilled plated through holes are located every .150”, centered between the edge of IST test circuit and the coupons routed profile.

Each plated through hole is designed to connect to only ONE of the internal reference planes. The first hole will be connected to the first reference plane by drilling directly through the copper plane (no pad is necessary), all remaining reference planes will have a .060” clearance (in the same x/y location).

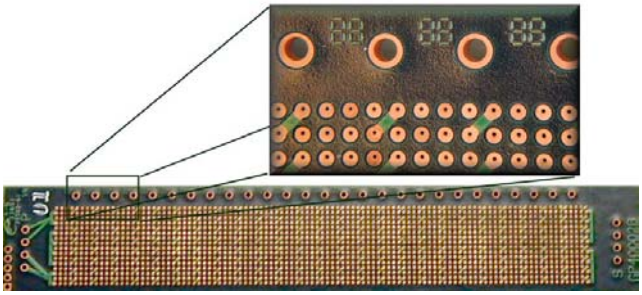
The following (second) hole will be connected only to the second internal reference plane; again all remaining planes will have a clearance (in the same x/y location). This process will be repeated for all internal reference planes.

For additional information related to the inclusion of capacitance (DELAM) vias into the coupon, see “instructions.pdf” included with each Generic IST design file.

Contact PWB Interconnect Solutions for further details on adding DELAM vias to existing coupon designs.

Figure 4 below illustrates an IST coupon with a close-up of the DELAM vias.

Figure 4 IST Test coupon + Capacitance Vias



NOTE:
PWB Interconnect is aware of other test equipment that operates on principles similar to those used by PWB. It is encouraged that alternative equipment or techniques be offered for consideration, in conjunction with their submission along with relevant test data. This test method will be revised as necessary to include these test systems as this information becomes available.